UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,852	03/12/2004	Isamu Miyanishi	2271/71532	2074

7590   08/04/2008

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EXAMINER
ZAMAN, FAISAL M

ART UNIT	PAPER NUMBER
2111	

MAIL DATE	DELIVERY MODE
08/04/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
Advisory Action ***Before the Filing of an Appeal Brief***	10/799,852	MIYANISHI ET AL.
	Examiner	Art Unit
	Faisal M. Zaman	2111

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED <u>17 July 2008</u> FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

   a) ☒ The period for reply expires <u>3</u> months from the mailing date of the final rejection.

   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

      Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will <u>not</u> be entered because

   (a)☐ They raise new issues that would require further consideration and/or search (see NOTE below);

   (b)☐ They raise the issue of new matter (see NOTE below);

   (c)☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

   (d)☐ They present additional claims without canceling a corresponding number of finally rejected claims.

      NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).

5. ☐ Applicant's reply has overcome the following rejection(s): _____.

6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

7. ☐ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
The status of the claim(s) is (or will be) as follows:
Claim(s) allowed: _____.
Claim(s) objected to: _____.
Claim(s) rejected: _____.
Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will <u>not</u> be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).

9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will <u>not</u> be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).

10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because:
    See Continuation Sheet.

12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____

13. ☐ Other: _____.

/MARK RINEHART/
Supervisory Patent Examiner, Art Unit 2111

Continuation of 11. does NOT place the application in condition for allowance because: Chu and Mirov teach all of the limitations of the argued claims, as discussed in the Final Office Action. With regards to Claim 22, Applicant argues that "the 16-bit register 320 of Chu ... is not a register circuit including a plurality of registers." However, the examiner has interpreted the "register circuit" to include both register 320 and register 332, since it can be seen that both of these registers receive information from HDC 312.

Also with regards to Claim 22, Applicant argues that the "LBA [logical block address] counter has nothing to do with specific addresses of the 16-bit data register 320 of Chu", and "the LBA counter of Chu is used to store the starting address of the data in the memory 420." The examiner disagrees. Contrary to Applicant's argument, the LBA counter of Chu does in fact store the addresses of the corresponding registers in the register circuit (i.e., the addresses in which the read data will be stored after it is buffered). The LBA counter is "used to store the starting address of the data" (paragraph 0038). Since the data which is intended to be sent to the host 10 is stored in the data register 320, the logical block addresses that are stored in memory 420 do in fact point to the "specific addresses of corresponding specified registers (i.e., register 320) in the register circuit".

Finally with regards to Claim 22, Applicant argues that "the state machine 400 of Chu ... does not perform an information writing operation for writing the first information and the second information into the first and second memory, respectively, in chronological order of access executed." The examiner disagrees. Contrary to Applicant's argument, the state machine 400 does in fact store the first information (i.e., the logical block address of register 320) in the first memory (i.e., memory 420) and the second information (i.e., data that is being read from the optical disk 360) into a second memory (i.e., the read data buffer within memory 420). Furthermore, it is stated in Chu that if a cache hit does not occur upon receiving a read request, the state machine 400 awakes the HDD 300 and writes the appropriate read data into the memory 420, see paragraph 0036. Therefore, it is clear that state machine 400 writes data into the appropriate locations in chronological order of access executed since it retrieves data from the disk in the order in which the read commands were received from the host 10.

With regards to Claim 19, Applicant argues that "Chu ... does not disclose or suggest a path selection controller configured to control the buffering circuit block to select the second data transfer path on an exclusive basis when the operation mode is changed from the regular operation mode to the low power consumption mode...". The examiner disagrees. Contrary to Applicant's argument, the state machine 400 (equated to the claimed "path selection controller") in Chu does in fact select between utilizing a write data buffer (i.e., the "second data transfer path") and not utilizing the write data buffer (i.e., the "first first transfer path"). In paragraph 0033, lines 1-5, Chu discloses that the state machine 400 only configures memory 420 to include a write data buffer when the system is in eData mode (i.e., a low power consumption mode). Accordingly, since the write data buffer within memory 420 is equated to the claimed "memory", it is clear that the state machine 400 selects between using the "memory" and not using the "memory" (i.e., can select between the two claimed data transfer paths) based on the type of power consumption mode the system is currently operating in (i.e., normal or eData mode).

Therefore, the claims stand as previously rejected.